

# Performance<sup>3</sup>

## The new VC Z series with **LINUX**® OS.

Based on a dual-core processor ARM® Cortex®-A9 with 866 MHz and an integrated FPGA the models of the new VC Z series offer solutions at extreme high-speed in real-time. The operating system VC Linux provides for the ideal interaction of hard- and software.

All cameras are equipped with a battery backed real-time-clock and come with up to 12 inputs and outputs, with trigger input and flash trigger output, as well as an Ethernet interface. 5 different CMOS sensors with global shutter and a resolution up to 4.2 Megapixel are available with all models.



### VC SBC nano Z series

- Interfaces: Gbit Ethernet, serial interface, 1 x I<sup>2</sup>C, 12 programmable I/Os, 1 trigger input (opto isolated), 1 flash trigger output
- Dimensions: 40 x 65 mm
- Also available with 1 and 2 remote image sensor boards

### VC nano Z series

- Interfaces: 100 Mbit Ethernet, I/Os: 2 inputs, 4 outputs, 1 trigger input, 1 flash trigger output. Pin connections and cables are compatible with VC nano models.
- Dimensions: 80 x 45 x 20 mm

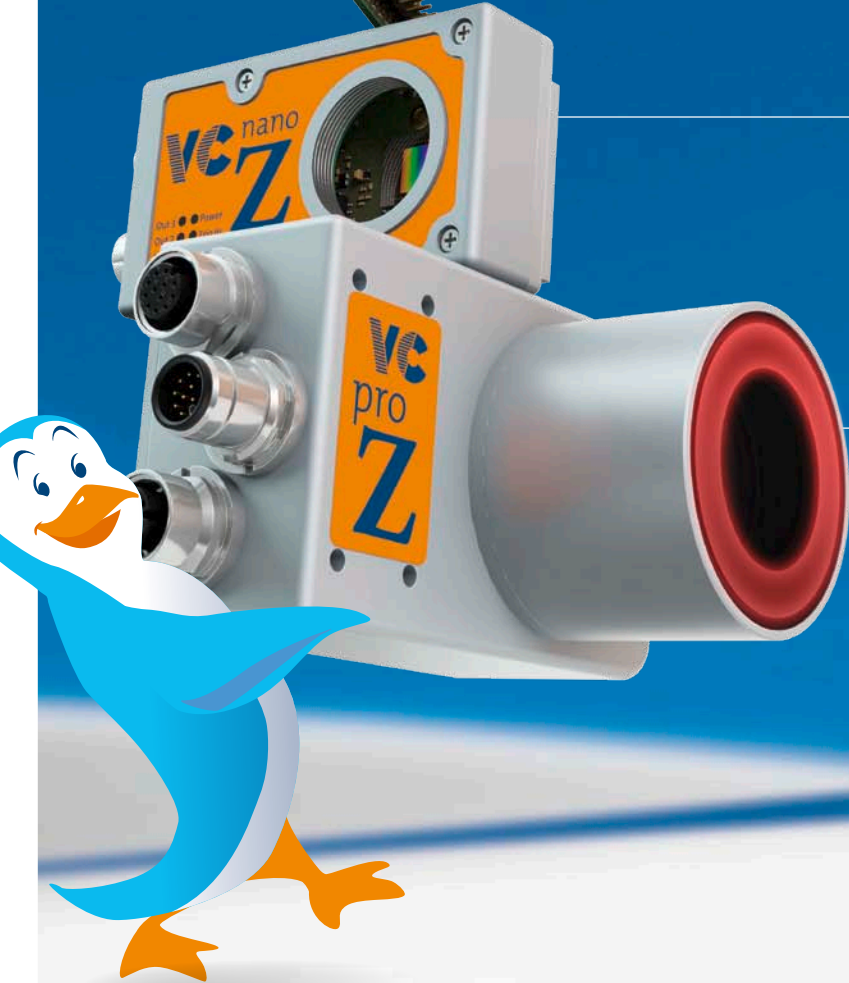
### VC pro Z series

- Interfaces: Gbit Ethernet, Encoder, 2 x external lighting, 4 inputs, 4 outputs, 1 trigger input, 1 flash trigger output, serial interface
- Dimensions: 90 x 58 x 36 mm
- Protective housing class IP67, M12 connectors
- Optional: lens, integrated lighting, autofocus module

Delivery starting from Q1/2015

**LINUX**  
inside

**FPGA**  
power



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**VC** VISION  
components®

# Three in one sweep: VC Lib, VC Power Lib, VC FPGA Packs.

The VC tools meet  
all requirements.



## VC Linux & VC Lib

(free of charge)

**VC Linux**, the new operating systems, and **VC Lib**, the extensive library containing the basics for image processing tasks, constitute the core of the new cameras. VC Linux provides for the ideal interaction of hard- and software and VC Lib concentrates 30 years of Know-how in machine vision.

Speed



FPGA  
Power



## VC FPGA Packs

(available from Q2/2015)

Each particular FPGA pack processes the requested function in hardware in parallel to image acquisition. With this enormous high-speed analysis is generated.

- **Smart Finder Pack:** Implementation in FPGA allows for enormous high-speed pattern matching tasks.
- **Edge & Filter Pack:** Implementation in FPGA of several functions.
- **VC Solution Pack:** Implementation of customer's FPGA routines.

## VC Power Lib

The VC Power Lib accelerates the processing of VC Lib functions by a factor of 3 in average, up to a factor of 10.

### Utilization ratio of FPGA in %\*

| Function         | BRAM | DSP48 | FF   | LUT  |
|------------------|------|-------|------|------|
| Sobel            | 1,7  | 0     | 1,1  | 4,0  |
| Pyramid          | 0,8  | 0     | 0,4  | 1,7  |
| Median 3x3       | 1,7  | 0     | 1,1  | 3,9  |
| Histogramm       | 1,7  | 0     | 0,6  | 2,0  |
| Canny Edge       | 6,7  | 1,3   | 3,4  | 15,9 |
| Pattern Matching | 43,2 | 0     | 10,2 | 34,5 |

\*In relation to the chip's total size.



## Customized Solutions + Projects

Project programming on customer-specific request: Software modification, development of mass production systems incl. FPGA programming, feasibility studies, implementing OEM code, etc.

Ask us, together with you we develop your ideal solution!



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